

# Hardware Users Guide

## High Speed, Low Power Analog-to-Digital Converter Evaluation Kit

**EKIT01-HMCAD1051**  
**EKIT01-HMCAD1041**  
**EKIT01-HMCAD1050**  
**EKIT01-HMCAD1040**

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Figure 1: EVAL01-HMCAD1050/40 Hittite EasyBoard™



Figure 2: EVAL01-HMCAD1051/1041 Hittite EasyBoard™

## 1 Introduction

This Hardware Users Guide describes the physical components of the EVAL01-HMCAD1051/1041 and EVAL01-HMCAD1050/40 variants of EasyBoard™. These boards are a part of the EKIT01-HMCAD1051/1041 evaluation kits. The kits consist of a Hittite EasyBoard™ FMC (FPGA Mezzanine Card) daughter board, a Xilinx SP601 development mother board and the EasySuite™ software tool.

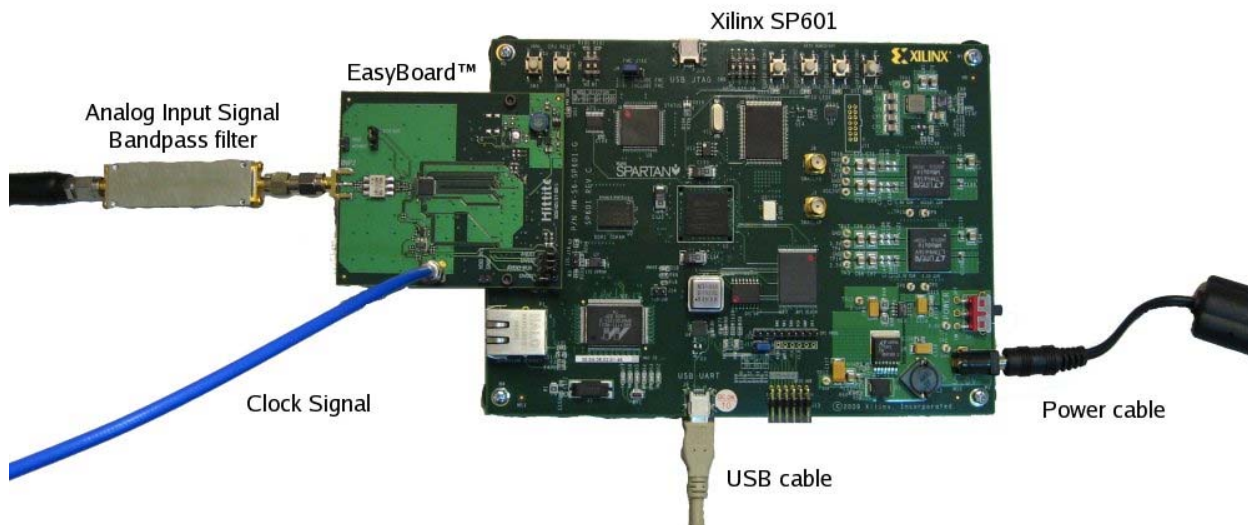
The EasyStack™ firmware is loaded on the Xilinx development board, which enables the configuration of the ADC and capture of data from the ADC.

All EasyBoards features Power Monitoring and Supply Voltage Adjustment.

## 2 Installation of Evaluation Kit

To use the Evaluation Kit, the following components are required:

- EVAL01-HMCAD1051/1041/1050/1040 EasyBoard™ (included in the kit)
- SP-601, Xilinx development board with EasyStack™ (included in the kit)
- Clock source
- Signal source
- PC with EasySuite™ software tool installed (software included in the kit)



Refer to Software Users Guide for EasySuite™ for installation of the EasySuite™ software.

## 3 Analog Inputs

### 3.1 Signal Quality

The quality of the input signal is the most important criterion to obtain good measurement results. The following points must be taken into consideration.

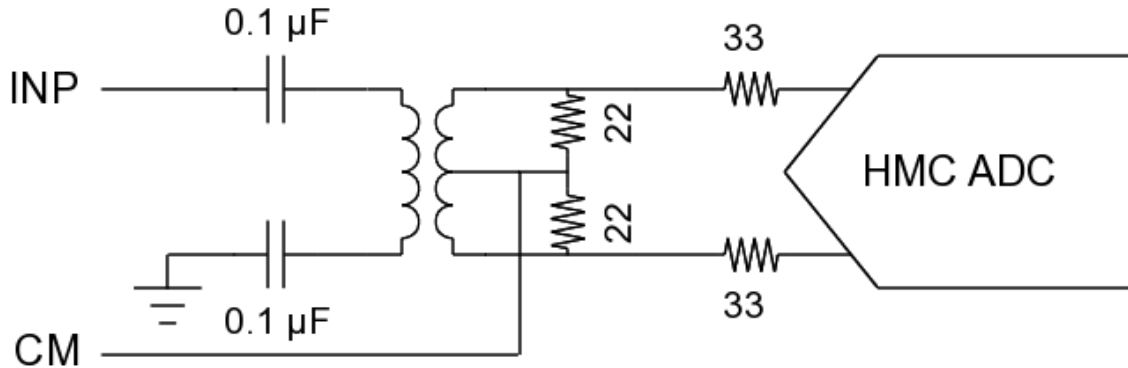
Apply a bandpass filter between the signal source and the EasyBoard™ RF input (INP1 thru INP4). This is required to obtain sufficiently low white noise levels and to reduce harmonic components from the signal source. Excellent results have been obtained with the TTE ([www.tte.com](http://www.tte.com)) filter series Q56T or KC4T. Make sure that large magnetic cores are used in the filters to avoid nonlinearity due to core saturation. Alternative vendors are K&L Microwave ([www.klmicrowave.com](http://www.klmicrowave.com)) and Allen Avionics Inc. ([www.allenavionics.com](http://www.allenavionics.com)). The input signal (after filtering) could be checked with a spectrum analyzer to ensure that noise and harmonic levels are significantly better than the theoretical contribution from the ADC.

**Make sure that the filter is located close to the connector as shown on the picture above. For these evaluation boards a long cable will significantly impact performance.**

Select a signal source with low noise and low phase noise. Excellent results are obtained with the Agilent E8663.

### 3.2 Analog input network

The input network of the EasyBoard™ is configured with an AC coupled transformer. This transformer converts the single ended input to a differential input for the ADC.



### 3.3 Clock Generation

The clock inputs on the HMCAD110X ADCs accept CMOS, LVDS, LVPECL and sine wave inputs. Connect a clock source to the SMA connector named CLK. The EasyBoard™ clock network is an AC coupled balun configuration with a 20MHz lower frequency limit. The network will accept a single ended sine wave or square wave input.

For best possible performance it is very important that the clock source have low jitter. Poor jitter performance will directly result in reduced SNR. The SNR contribution from jitter is given by equation (1) assuming a full scale input signal at frequency,  $f_{IN}$ , and TRMS-jitter, measured in second Root-Mean-Square.

$$(1)$$

One can see that a 1ps clock jitter with a 25 MHz full scale input signal results in an additional SNR component of 76 dBc. Because of this the clock signal should be treated with the same care as the analog inputs to the ADC.

It is possible to reconfigure the board to accept a clock generated directly from the FPGA or from a clock generator located on the Xilinx Spartan-6 evaluation board.

Contact [adc@hittite.com](mailto:adc@hittite.com) for instructions on how to reconfigure the board.

## 4 Jumpers and connectors

### 4.1 Power domains

JP4/JP5 in lower right corner, see section 11.1, must be set to enable power for all power domains to the converter. There should be one jumper on each row, either to the right or the left. Setting the jumper to the right, will include that power domain in the built in current measurement feature. Setting the jumper to the left, the current measurement for that domain will be bypassed.

All the power domains except OVDD are on the 1.8 V power supply. They are separated on the board so that it is possible to measure the current consumption individually for each power domain on the chip. The domains are as follows:

- AVDD is the analog power domain and includes all power consumption in the ADC cores.
- DVDD is the digital power domain and includes power consumption in the digital block and the LVDS IO drivers.
- AVDD\_AUX is the power domain for the reference circuit.
- OVDD is the domain for the IO ring on the pads inside the chip. This domain drives the CMOS outputs. See section 4.2 for more details.

### 4.2 CMOS data output

The data output is in CMOS format and the logical level is controlled by the OVDD power domain. It is possible to select either 1.8 V or 2.5 V as voltage level for the CMOS output. Setting the jumper for the OVDD domain (the bottom one) to the left will select 2.5 V mode. Setting it to the right will select 1.8 V mode, and it will be included in the current meter circuit.

Using 1.8 V for the OVDD domain is not recommended for normal use, since 1.8 V is quite close to the threshold voltage for the 2.5 V CMOS input on the FPGA.

### 4.3 Common mode

JP1, see section 11.1, selects the source for common mode drive. This is the common mode level for the differential input signals. If the jumper is placed in the top position, the common mode is driven by the ADC's common mode output. The drive strength of this output is programmable from the configuration software. See the datasheet for details around this drive strength.

If the jumper is placed in the lower position, the common mode is set by two on board 51 ohms resistors between the 1.8 V supply and ground. It is possible to override this common mode externally by connecting a voltage source to the terminal port JP2 in the lower left corner.

## 4.4 3.3 V supply output

Terminal JP6 offers a 3.3 V supply output. This supply originates from the power converters on the Xilinx mother board. It can drive a load up to around 5 A. This terminal can be used as a power supply for an external crystal oscillator, for instance RFPRO33-1000.000 from Crystek Corporation, which can be used as a clock source.

## 4.5 FMC connector

The FMC (FPGA Mezzanine Card) connector, J1, is located on the backside of the board. This is the low pin count version of the FMC connector. Connect this with the FMC connector on the Xilinx mother board.

# 5 Special features

## 5.1 Power monitoring

U9 is a power monitoring chip. This can measure the current consumption and voltage level for the ADC. See 4.1 Power domains for details about measuring different power domains on the ADC. If all jumpers on JP4/JP5 are placed to the right, the total power consumption of the chip is measured.

The EasySuite™ software controls and collects data from the monitoring chip.

If the power measurement gives unexpected results, try to bypass the OVDD domain from the power measurement circuit.

## 5.2 Supply voltage level

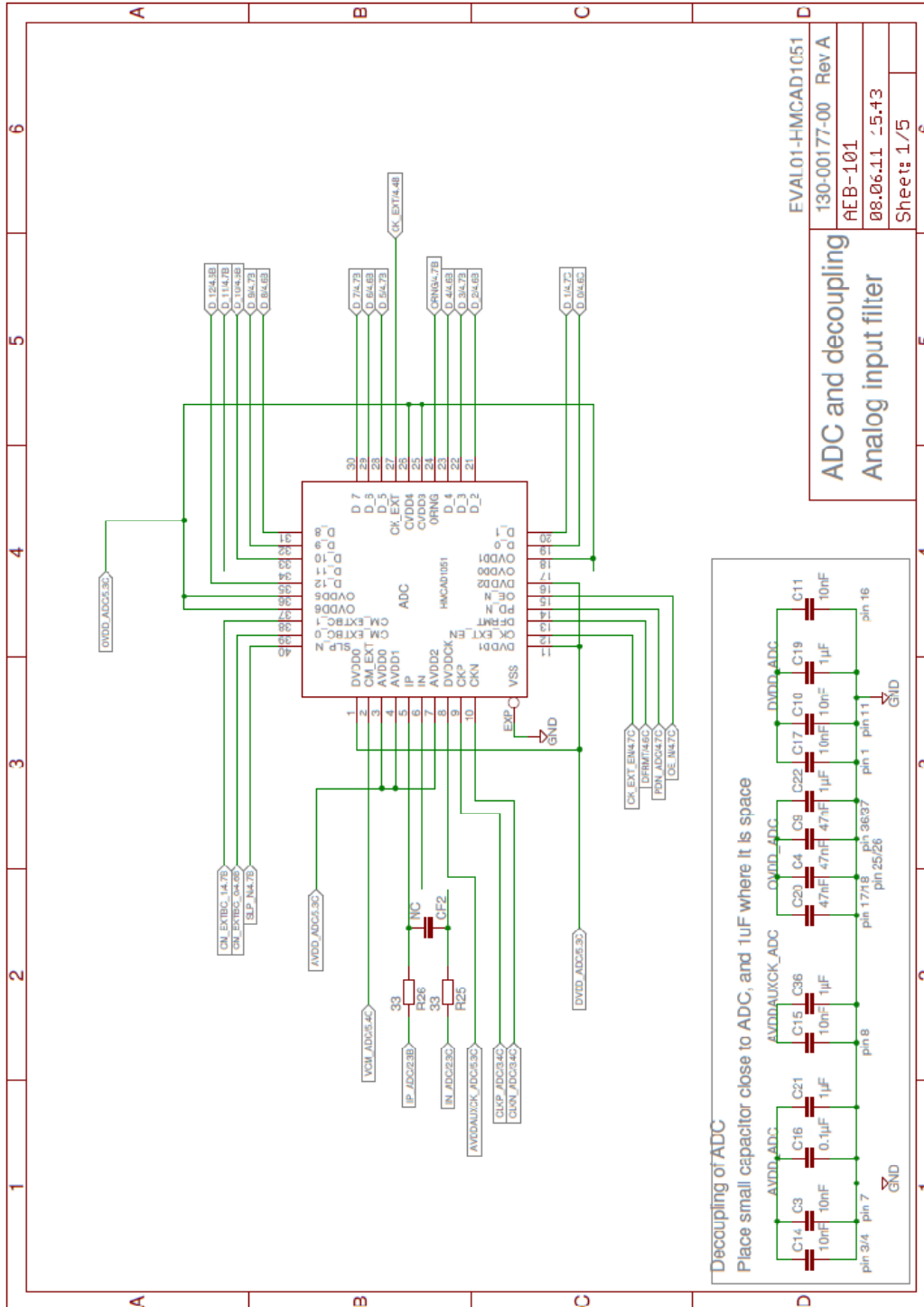
The supply voltage level for the ADC can be adjusted through the EasySuite software. U12 is a digital potentiometer which can adjust the supply level between 1.7 V and 2.0 V. Refer to the EasySuite™ Software Users Guide for an explanation of how to set the supply voltage.

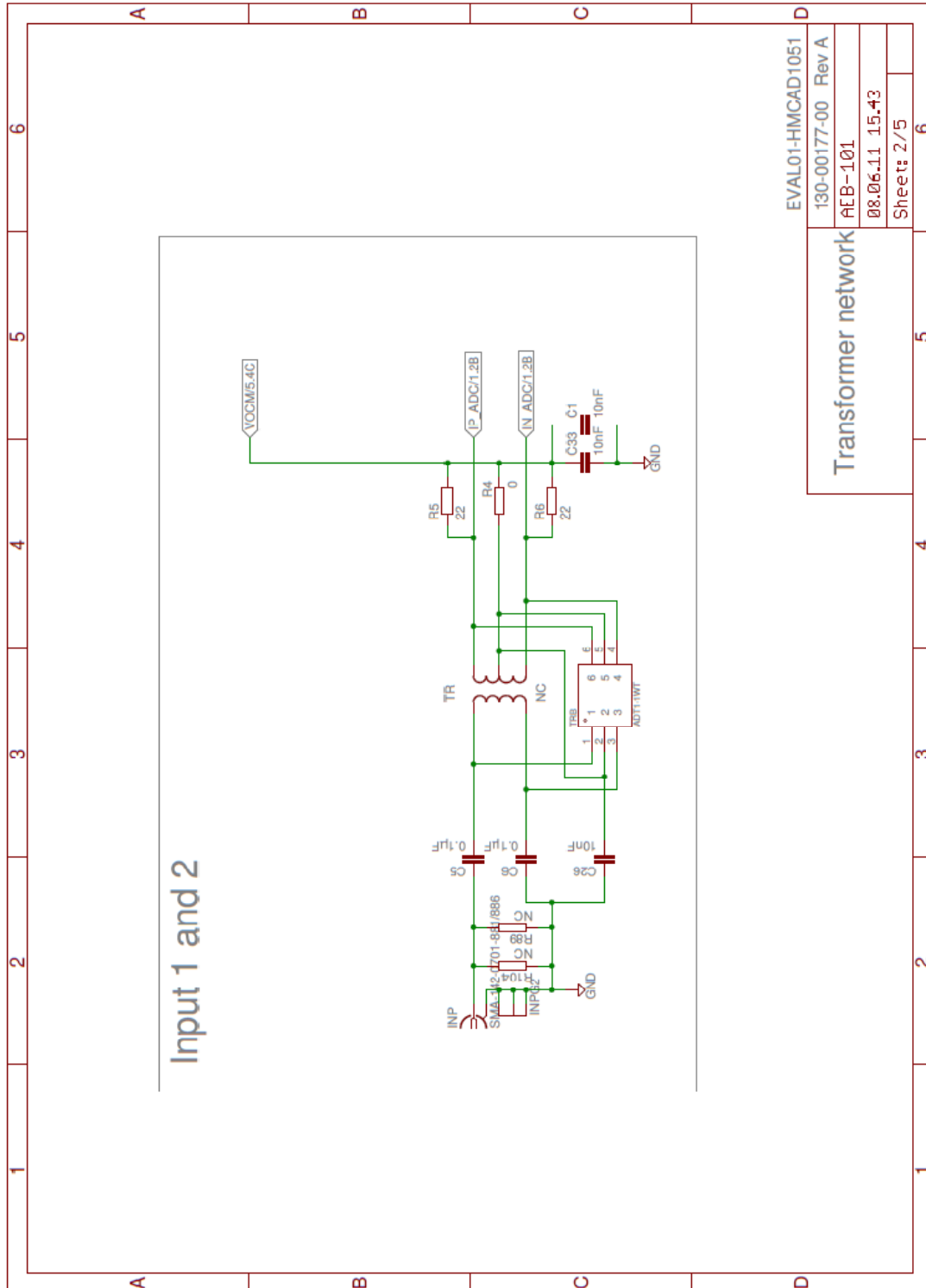
## 6 List of material for EVAL01-HMCAD1051

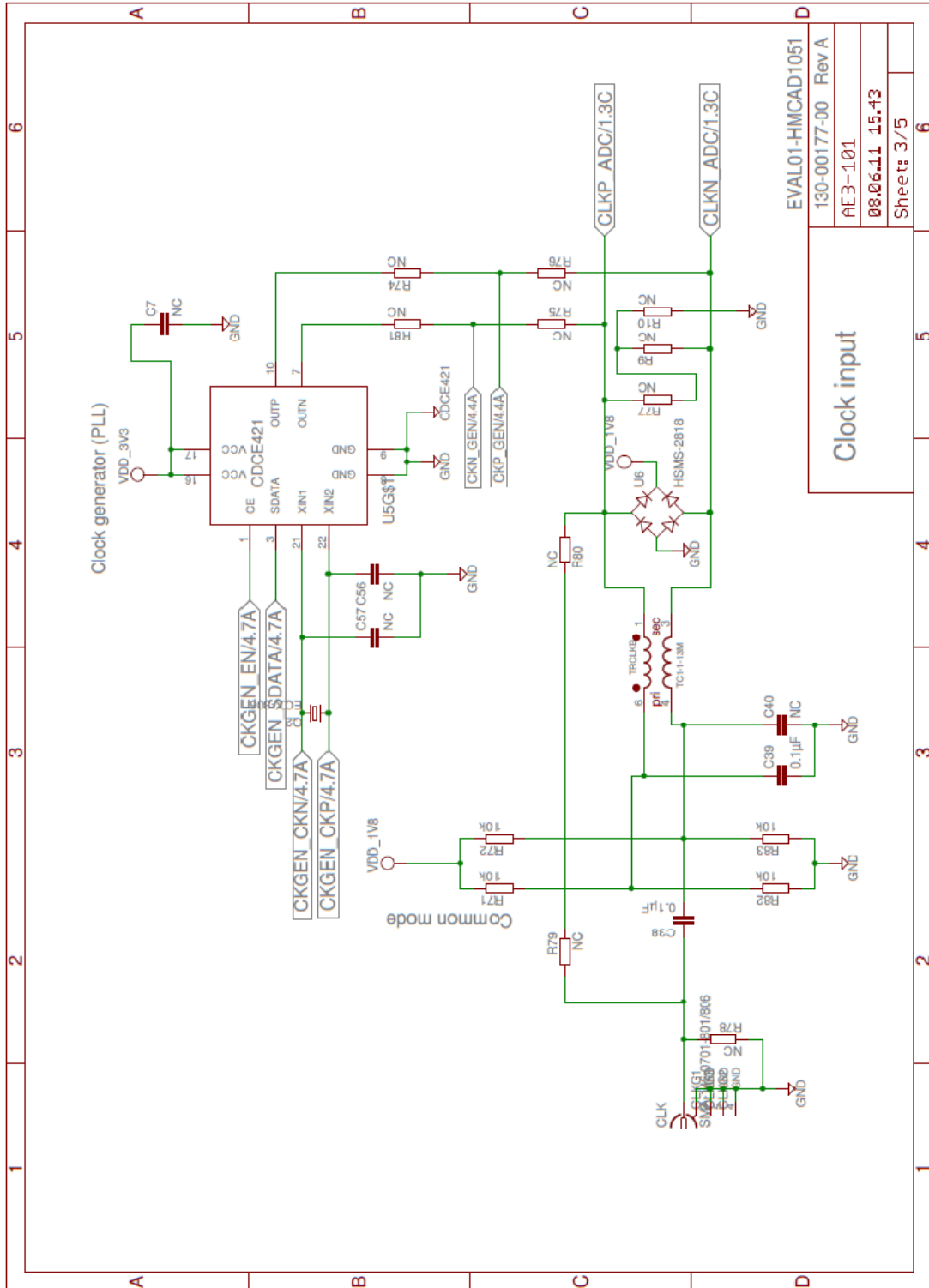
Qty	Refdes	Description
1	ADC	SINGLE 13/12-BIT 20 TO 65 MSPS A/D CONVERTER
1	CLK	CONN RECEPT STRAIGHT PCB .155" G
1	D1	RECT SCHOTTKY 30V 1.5A 3-2A1A
1	INP2	SCD, MA-F, EGDE LAUNCH, .031" BOARD, JOHNSON
1	J1	CONN SNGL-END ARRAY MALE 160POS
1	JP1	TERMINAL STRIP, SINGLE ROW 3 PIN .100", TRW
1	JP4	TERMINAL STRIP, SGL ROW 4 PIN TH .100", TLW
1	JP5	TERMINAL STRIP, DUAL ROW 2X4 TH .100", TLW
1	L4	INDUCTOR SHIELD PWR 3.3UH 7045
1	R90	RES 0.20 OHM 1/4W 1% 0805 SMD
1	R93	RES 100K OHM 1/10W 1% 0603 SMD
1	R96	RES 10.0K OHM 1/10W 1% 0603 SMD
1	TR2B	RF TRANSFORMER, 1:1, 0.4- 800 MHZ, ADT1-1WT+
1	TRCLKB	RF TRANSFORMER, 50 OHM, 4.5-3000MHZ, TC1-1-13M+
1	U10	IC REGULATOR BUCK 1.5A SOT23-5
1	U12	IC POT DGTL SPI 256POS SOT23-8
1	U6	Schottky Diode, RF, Bridge Quad
1	U9	IC CURRENT MONITOR 1% SOT23-8
2	C16,C49	CAP CERM .1UF 10% 50V X7R 0603
2	C50-C51	CAP CER 47UF 6.3V X5R 20% 0805
2	JP2,JP6	TERMINAL STRIP, SGL ROW 2 PIN TH .100", TLW
2	R1,R94	RES 20K OHM 1/10W 1% 0603 SMD
2	R25-R26	RES 33.0 OHM 1/16W 1% 0402 SMD
2	R29-R30	RES 100 OHM 1/10W 1% 0603 SMD
2	R5-R6	RES 22 OHM 1/16W 5% 0402 SMD
3	C4,C9,C20	CAP CERM 4700PF 10% 25V X7R 0402
3	R4,R86-R87	RES ZERO OHM 1/16W 5% 0402 SMD
4	C5-C6,C38-C39	CAP CER .1UF 50V 10% X7R 0402
4	R71-R72,R82-R83	RES 10K OHM 1/16W 5% 0402 SMD
5	R13,R15-R16,R91-R92	RES ZERO OHM 1/10W 5% 0603 SMD
7	C8,C13,C19,C21-C22,C36,C44	CAP CER 1UF 25V 15% X5R 0603
9	C1,C3,C10-C11,C14-C15,C17,C26,C33	CAP CER .01UF 50V 10% X7R 0402
27	C7,C40,C56-C57,CF2,Q2,R9-R10,R14,R17-R20,R74-R81,R84-R85,R89,R104,TR2,U5	DO NOT POPULATE COMPONENTS

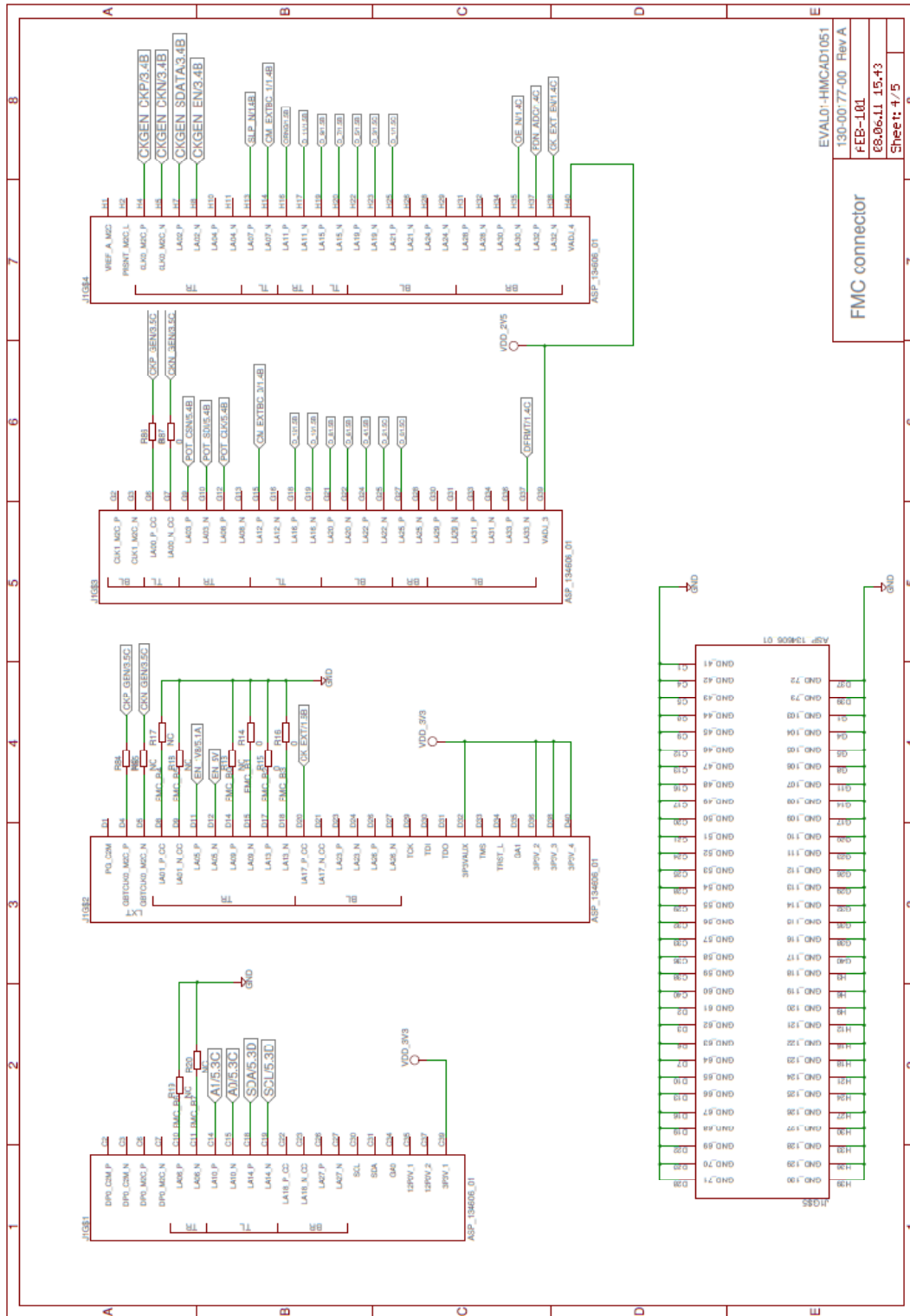


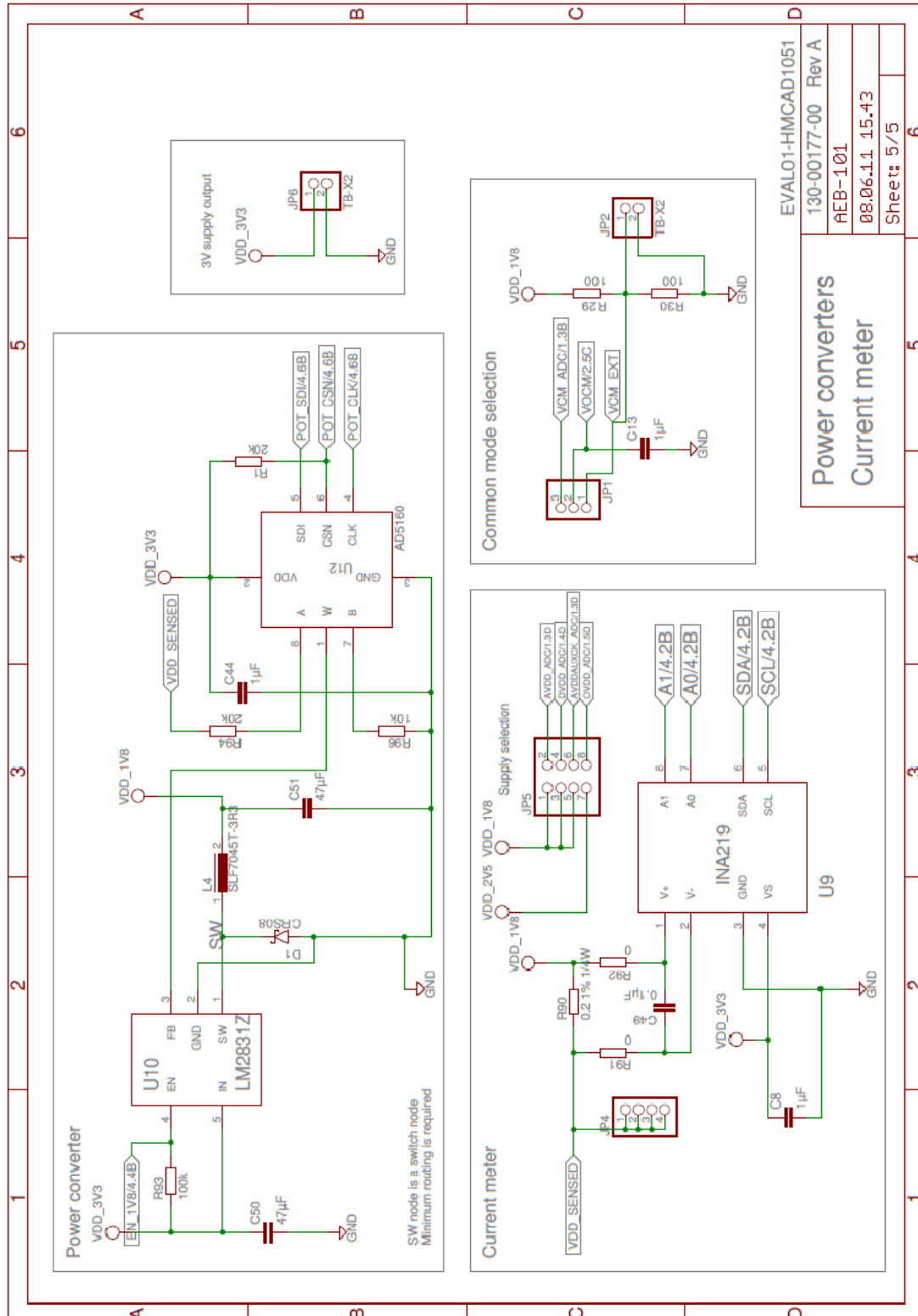
## 7 Schematics for EVAL01-HMCAD1051









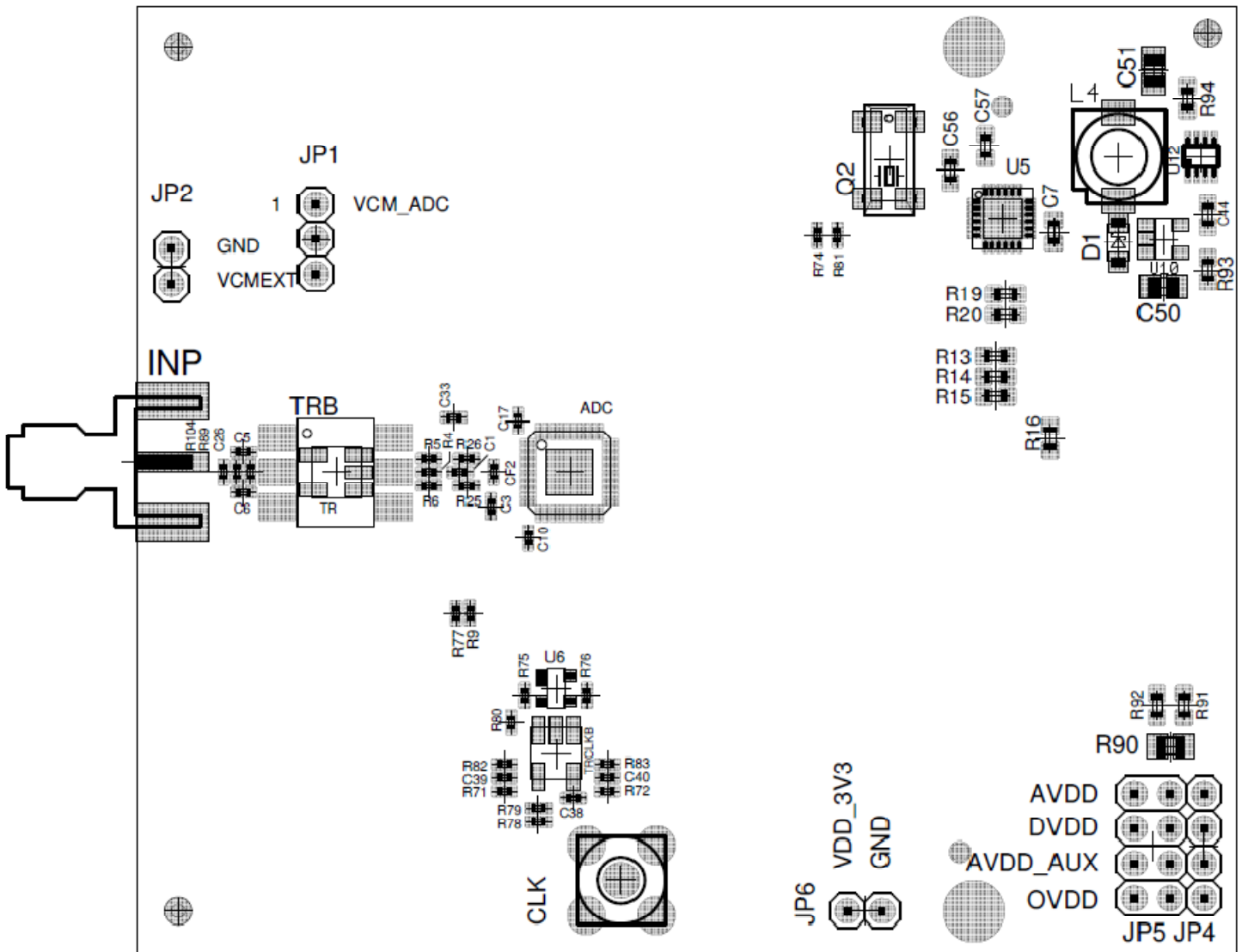


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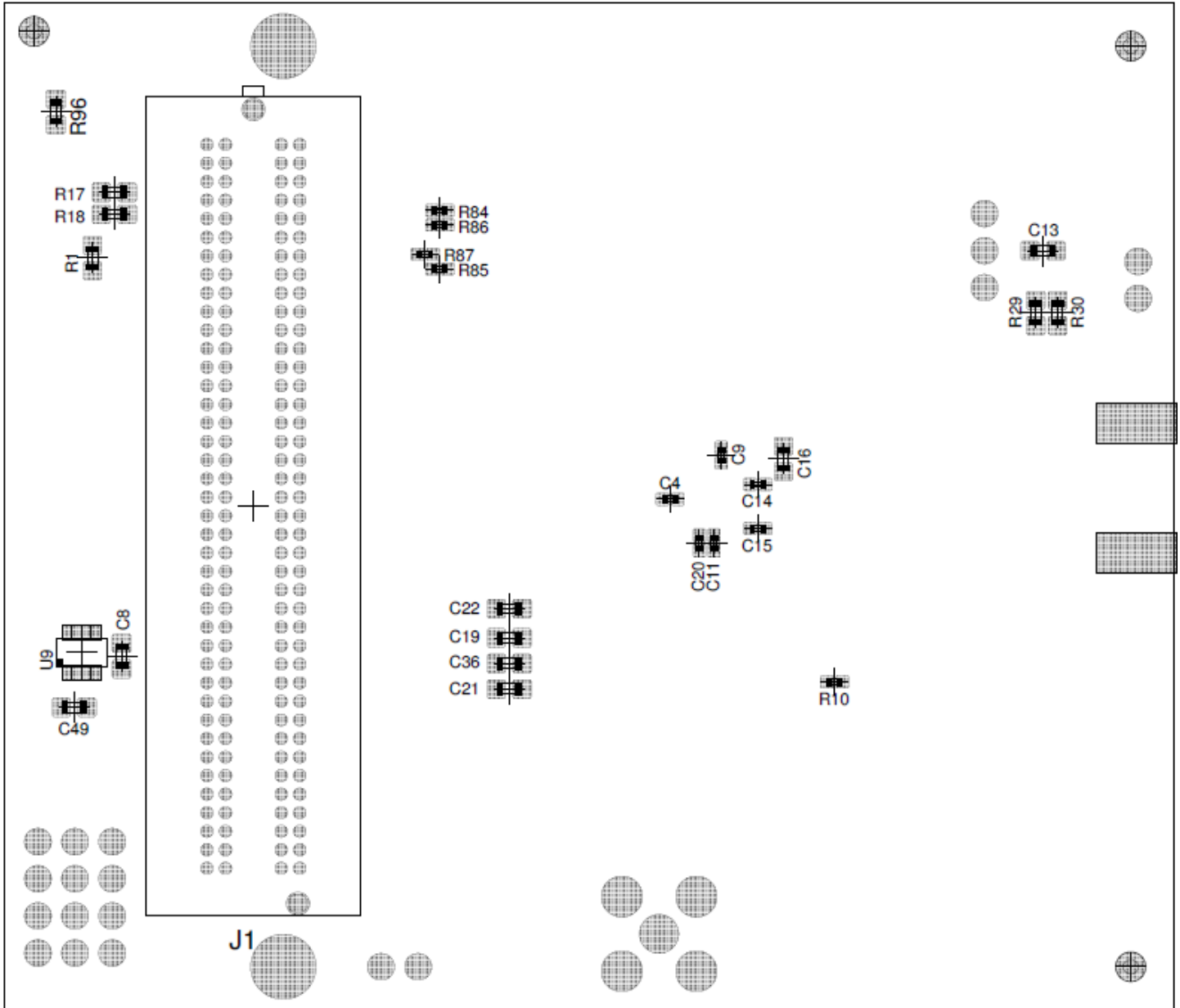
Power converters  
Current meter

## 8 Physical layout for EVAL01-HMCAD1051

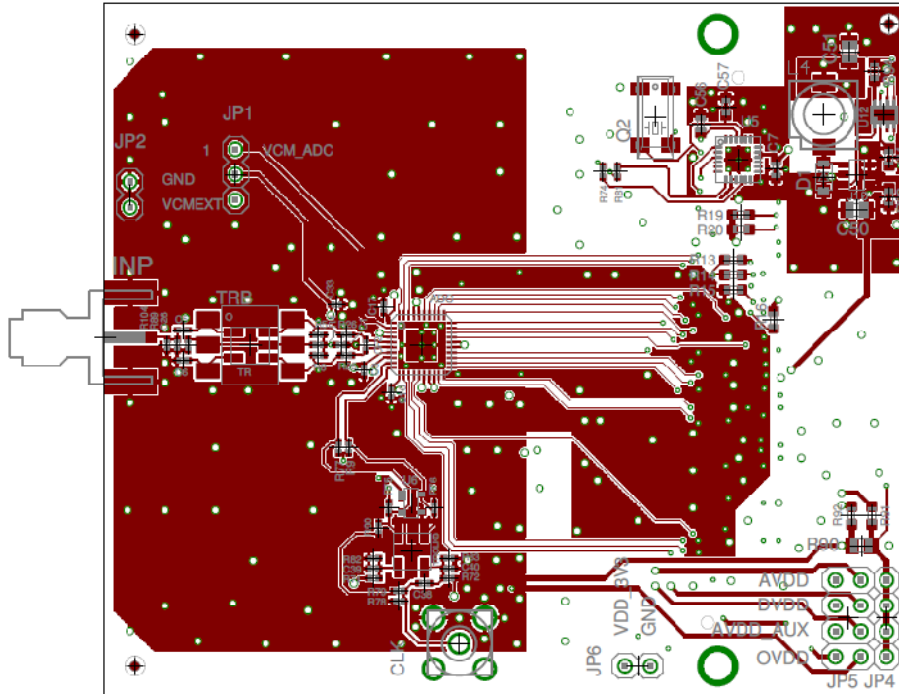
### 8.1 Component placement TOP



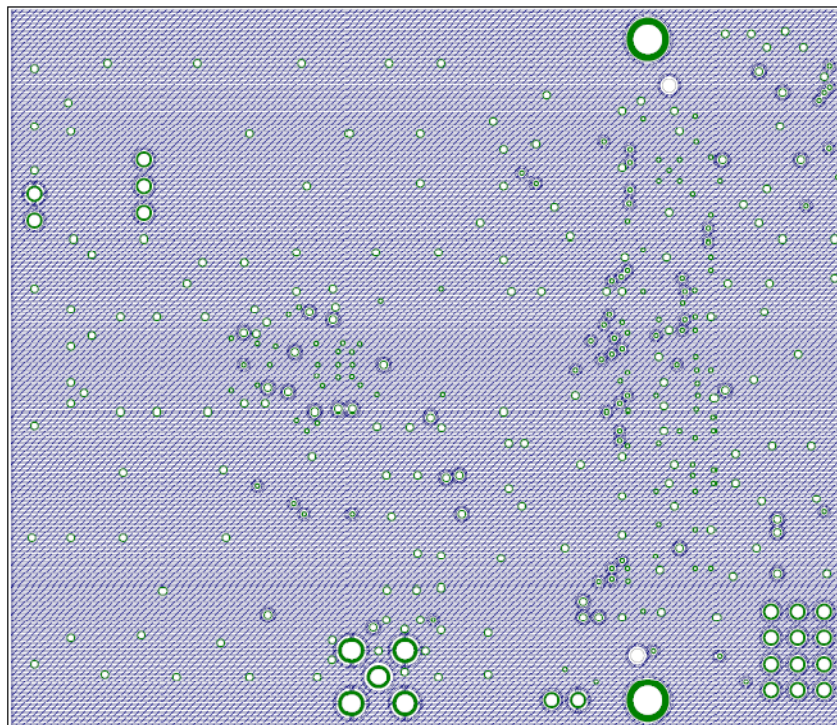
## 8.1 Component placement BOTTOM



## 8.2 Top layer

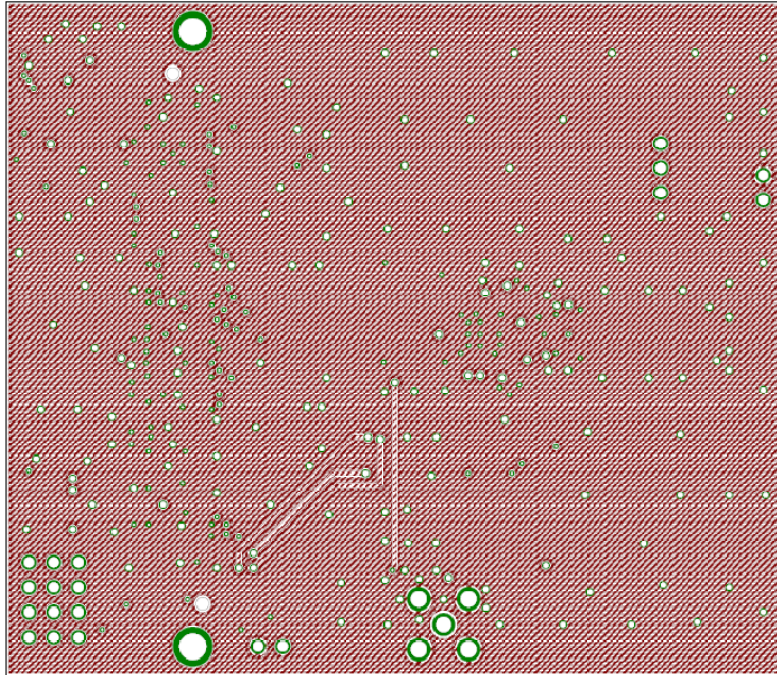


## 8.3 Inner layer top

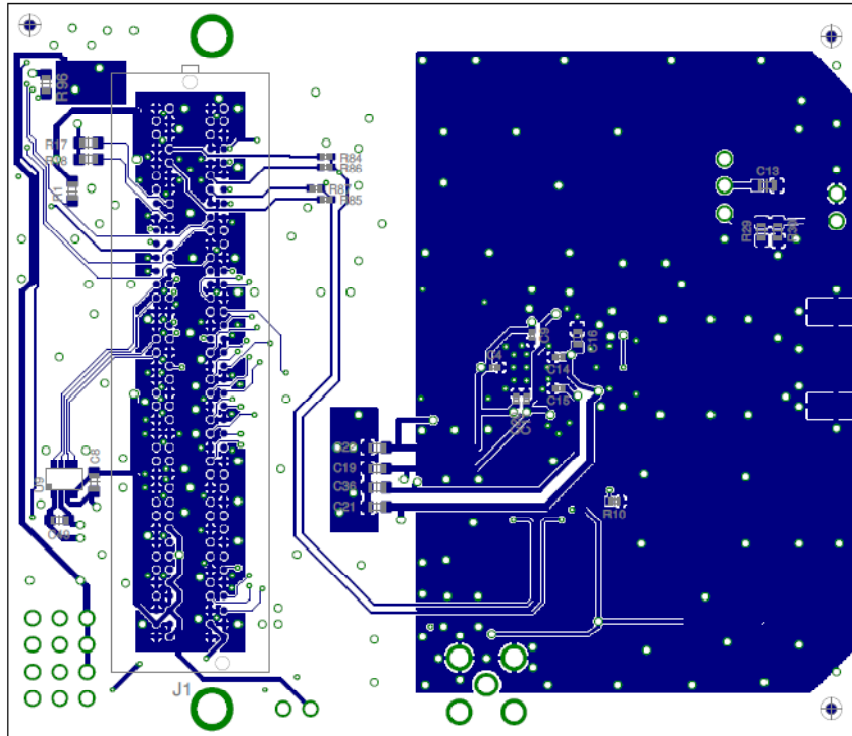




## 8.4 Inner layer bottom



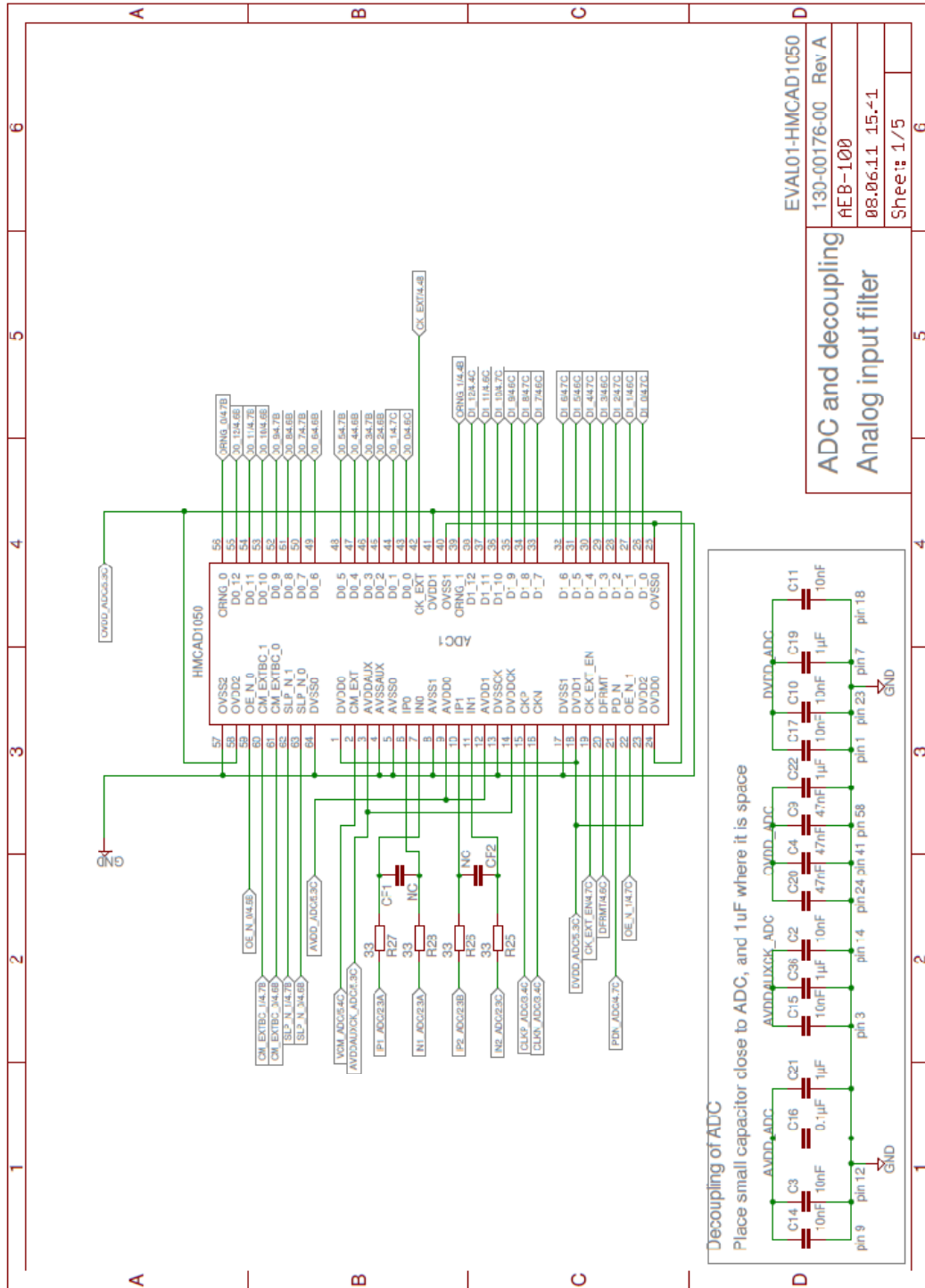
## 8.5 Bottom layer

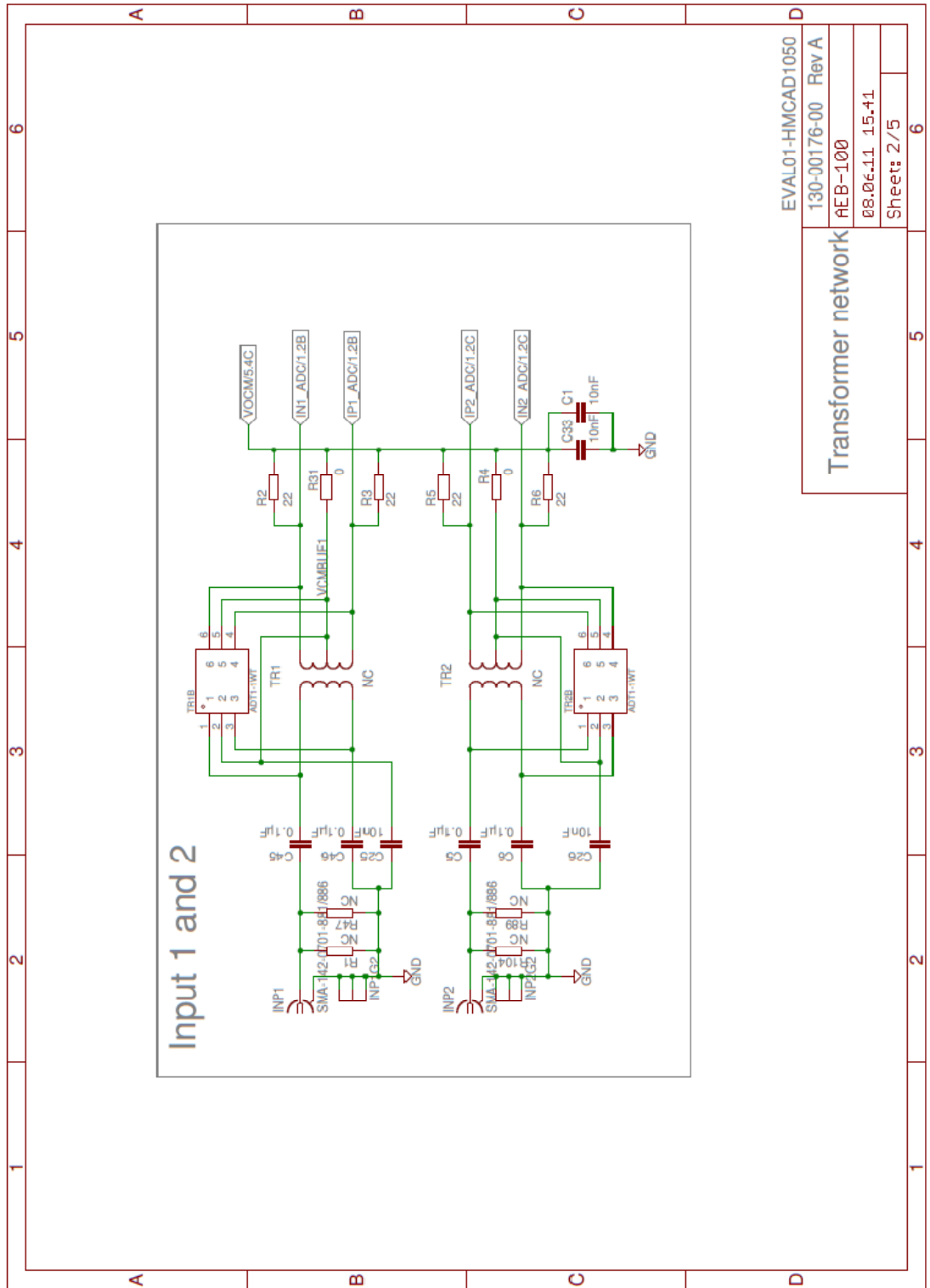


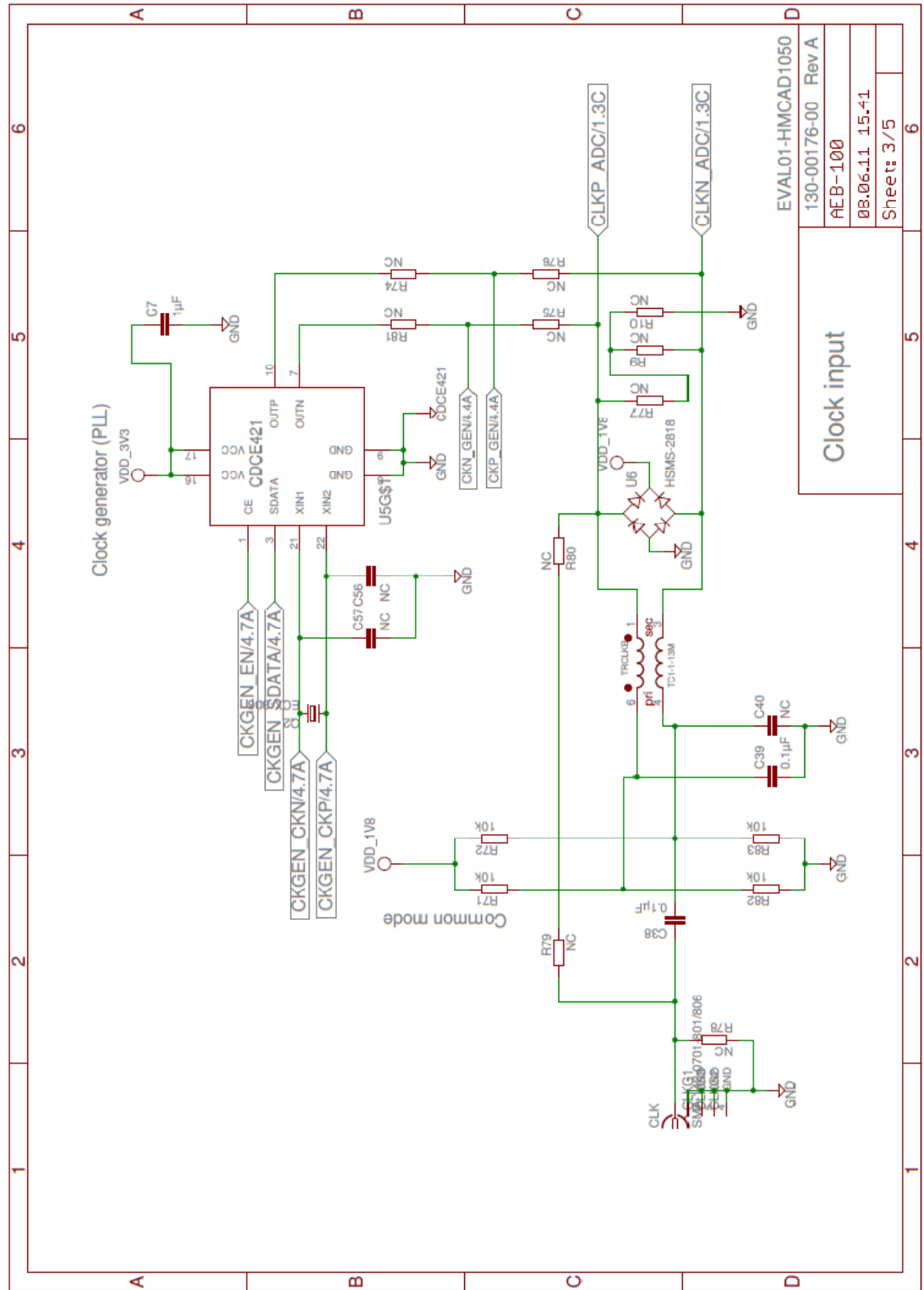
## 9 List of Materials EVAL01-HMCAD1050

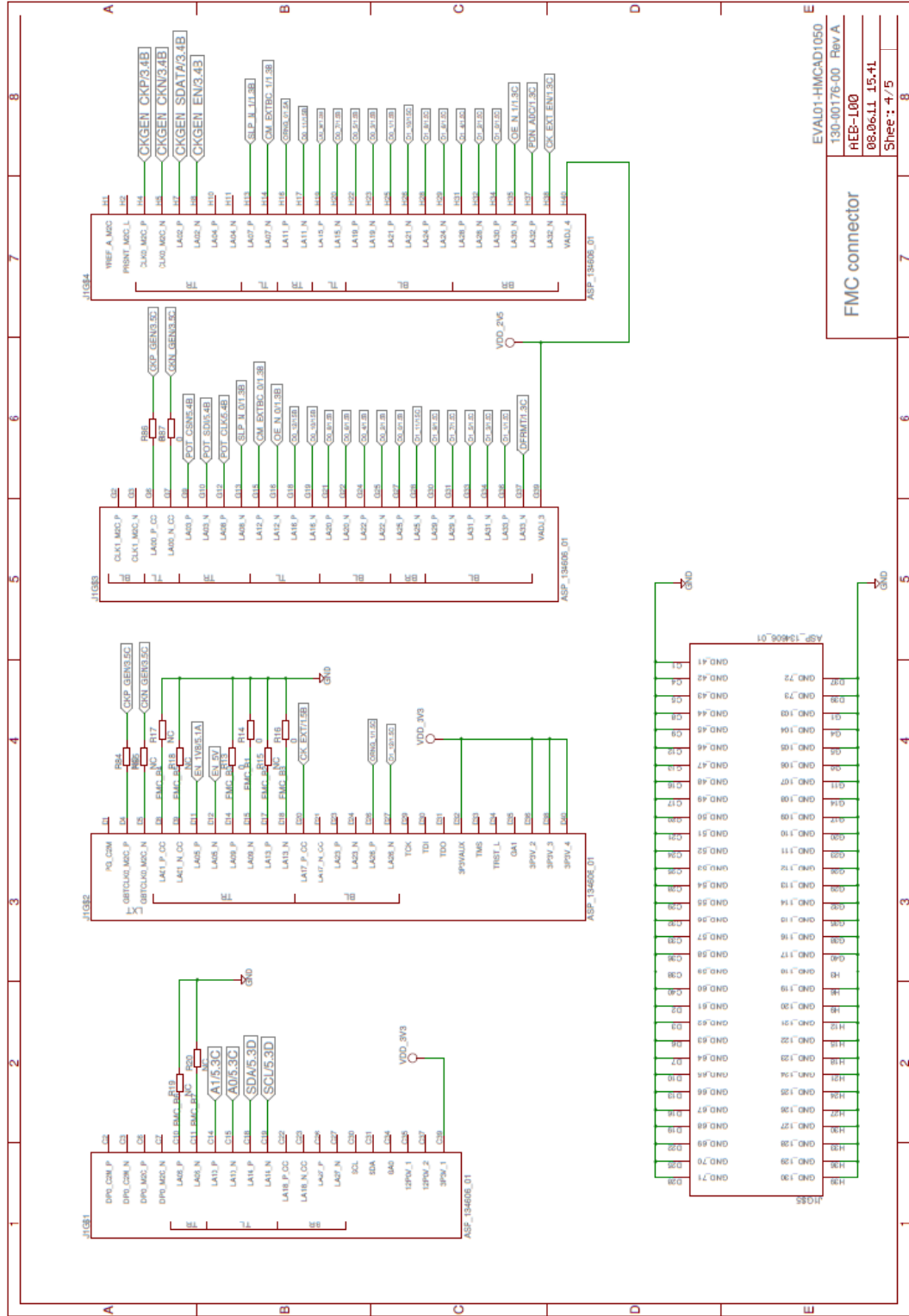
Qty	Refdes	Description
1	ADC1	DUAL 13/12-BIT 20 TO 40 MSPS A/D CONVERTER
1	CLK	CONN RECEPT STRAIGHT PCB .155" G
1	D1	RECT SCHOTTKY 30V 1.5A 3-2A1A
1	J1	CONN SNGL-END ARRAY MALE 160POS
1	JP1	TERMINAL STRIP, SINGLE ROW 3 PIN .100", TRW
1	JP4	TERMINAL STRIP, SGL ROW 4 PIN TH .100", TLW
1	JP5	TERMINAL STRIP, DUAL ROW 2X4 TH .100", TLW
1	L4	INDUCTOR SHIELD PWR 3.3UH 7045
1	R90	RES 0.20 OHM 1/4W 1% 0805 SMD
1	R93	RES 100K OHM 1/10W 1% 0603 SMD
1	R96	RES 10.0K OHM 1/10W 1% 0603 SMD
1	TRCLKB	RF TRANSFORMER, 50 OHM, 4.5-3000MHz, TC1-1-13M+
1	U10	IC REGULATOR BUCK 1.5A SOT23-5
1	U12	IC POT DGTL SPI 256POS SOT23-8
1	U6	Schottky Diode, RF, Bridge Quad
1	U9	IC CURRENT MONITOR 1% SOT23-8
2	C16,C49	CAP CERM .1UF 10% 50V X7R 0603
2	C50-C51	CAP CER 47UF 6.3V X5R 20% 0805
2	INP1-INP2	SCD, MA-F, EGDE LAUNCH, .031" BOARD, JOHNSON
2	JP2,JP6	TERMINAL STRIP, SGL ROW 2 PIN TH .100", TLW
2	R29-R30	RES 51 OHM 1/10W 1% 0603 SMD
2	R7,R94	RES 20K OHM 1/10W 1% 0603 SMD
2	TR1B,TR2B	RF TRANSFORMER, 1:1, 0.4- 800 MHZ, ADT1-1WT+
3	C4,C9,C20	CAP CERM 4700PF 10% 25V X7R 0402
4	R25-R28	RES 33.0 OHM 1/16W 1% 0402 SMD
4	R2-R3,R5-R6	RES 22 OHM 1/16W 5% 0402 SMD
4	R4,R31,R86-R87	RES ZERO OHM 1/16W 5% 0402 SMD
4	R71-R72,R82-R83	RES 10K OHM 1/16W 5% 0402 SMD
5	R13-R14,R16,R91-R92	RES ZERO OHM 1/10W 5% 0603 SMD
6	C5-C6,C38-C39,C45-C46	CAP CER .1UF 50V 10% X7R 0402
8	C7-C8,C13,C19,C21-C22,C36,C44	CAP CER 1UF 25V 15% X5R 0603
11	C1-C3,C10-C11,C14-C15,C17,C25-C26,C33 C40,C56-C57,CF1-CF2,Q2,R1,R9- R10,R15,R17-R20,R47,R74-R81,R84-	CAP CER .01UF 50V 10% X7R 0402
30	R85,R89,R104,TR1-TR2,U5	DO NOT POPULATE COMPONENTS

## 10 Schematics for EVAL01-HMCAD1050



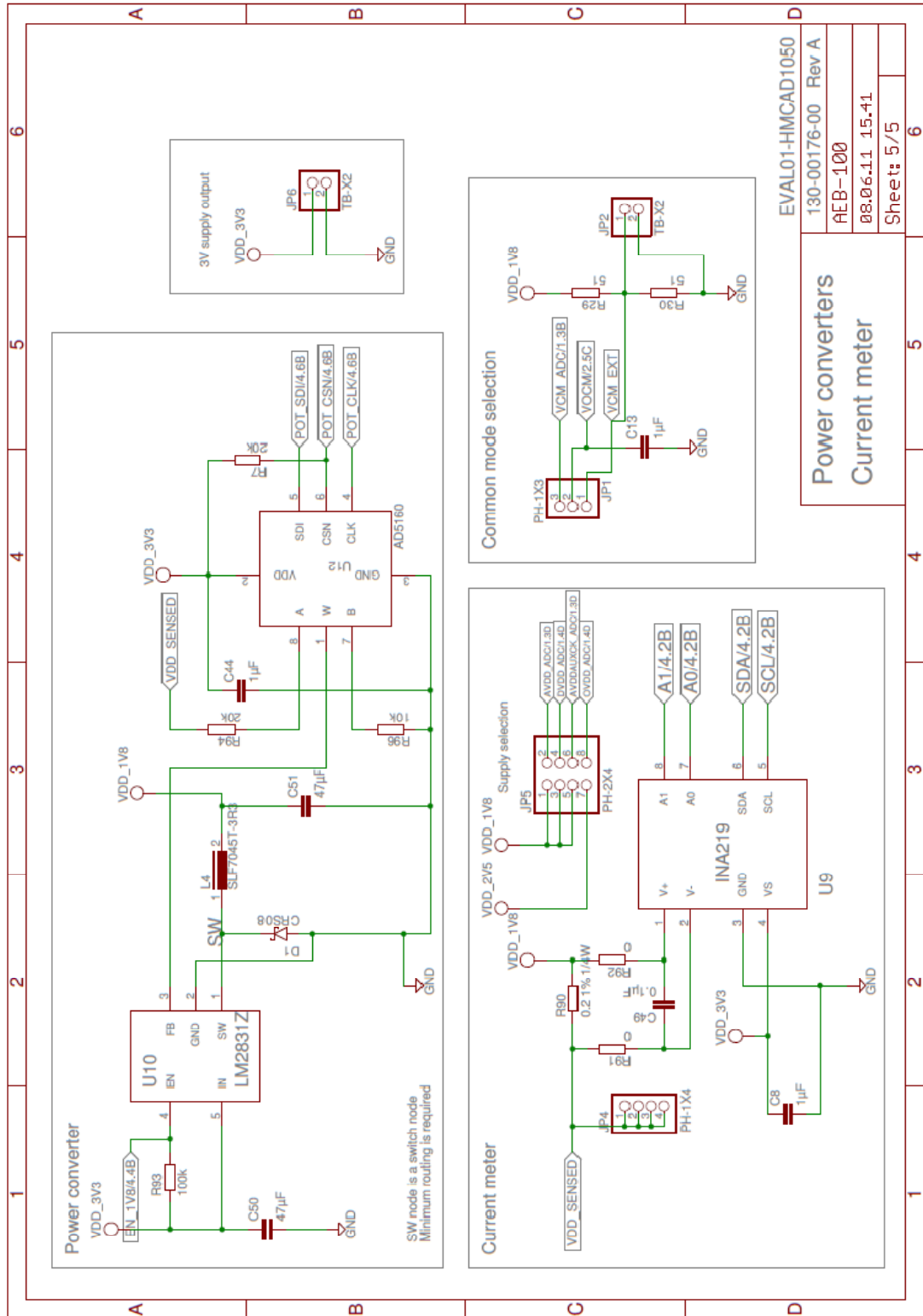






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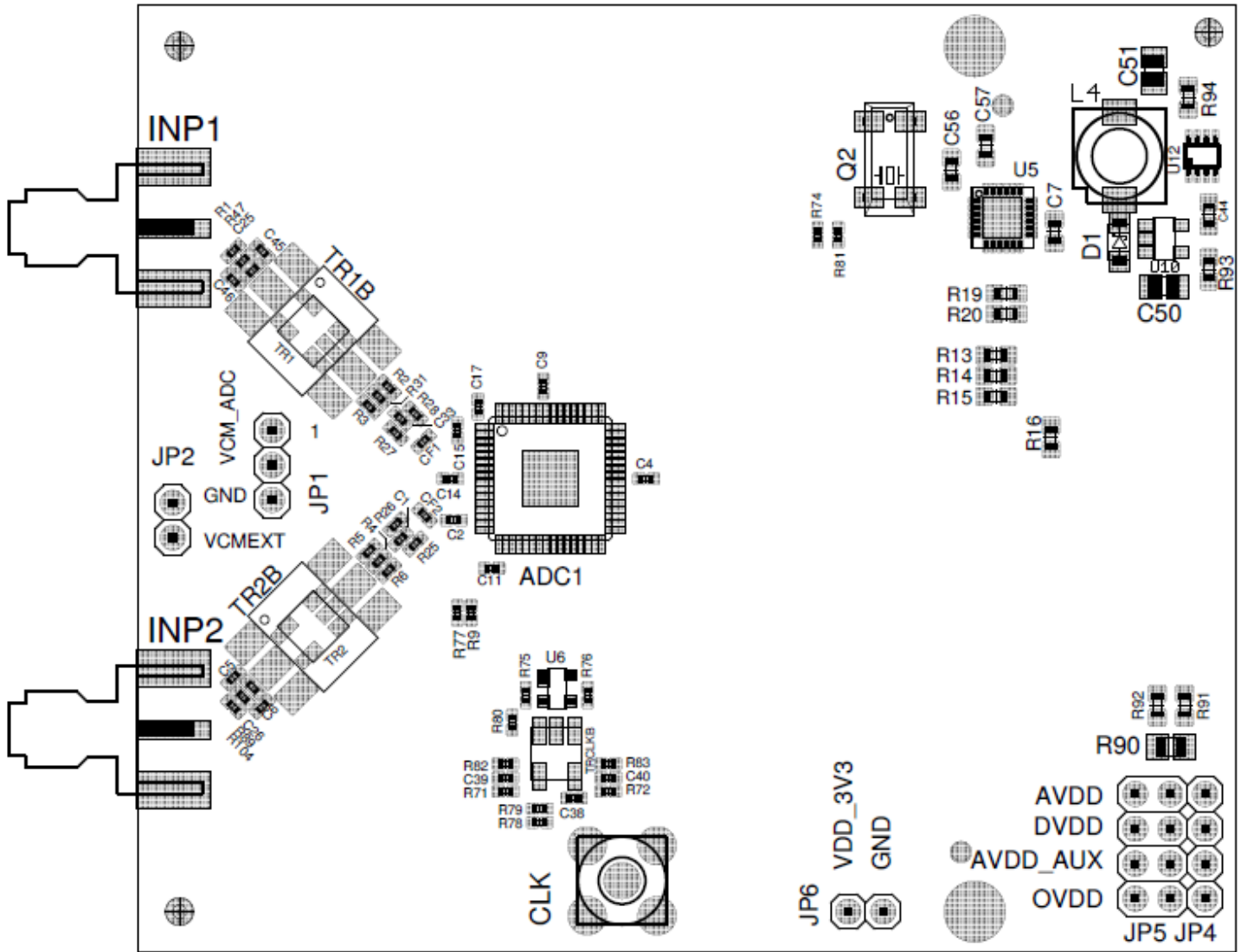
FMC connector



EVAL01-HMCAD1050	
130-00176-00	Rev A
AEB-100	
08.06.11 15.-41	
Sheet: 5/5	
Power converters	6
Current meter	6

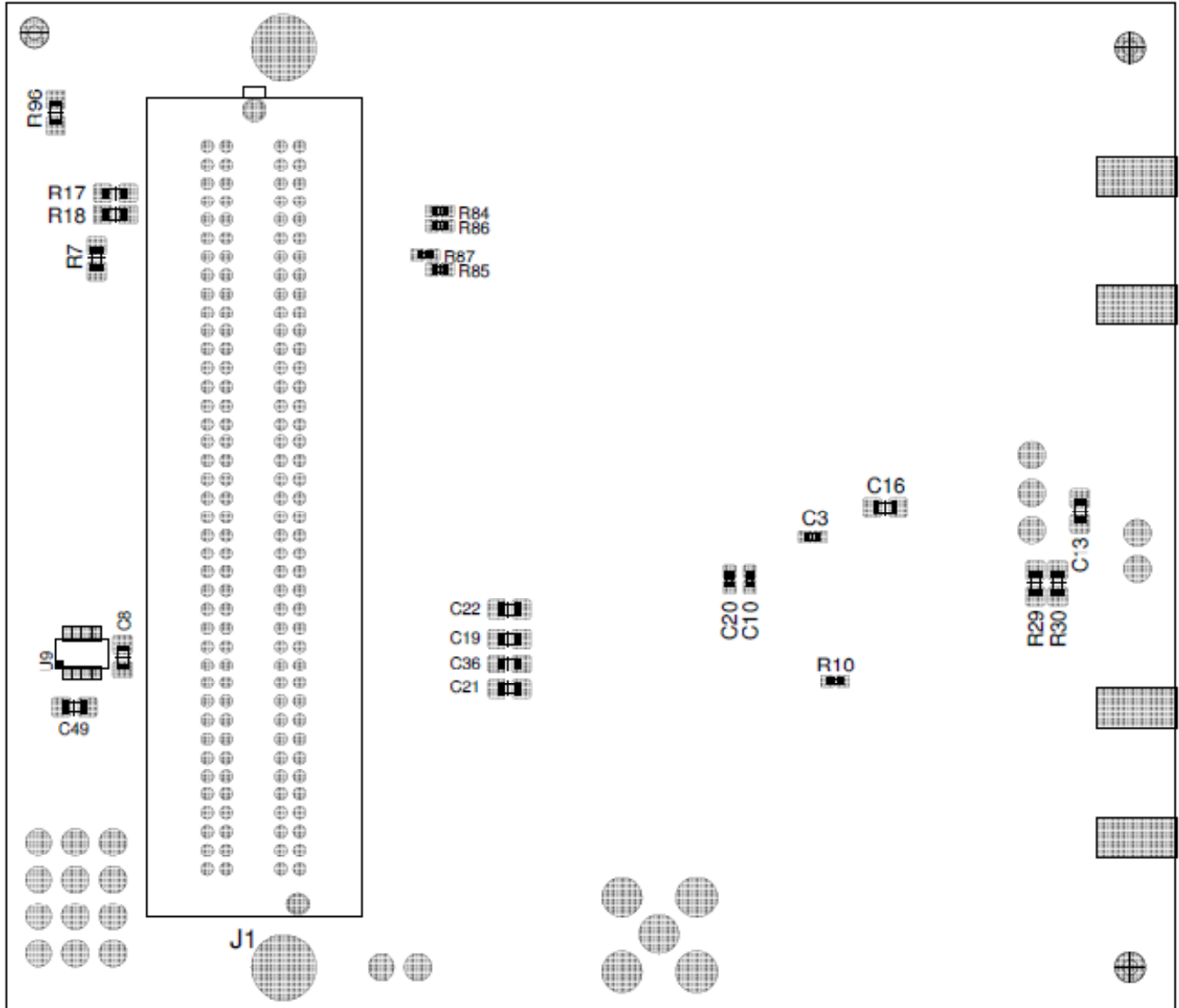
## 11 Physical layout for EVAL01-HMCAD1050

### 11.1 Component placement TOP

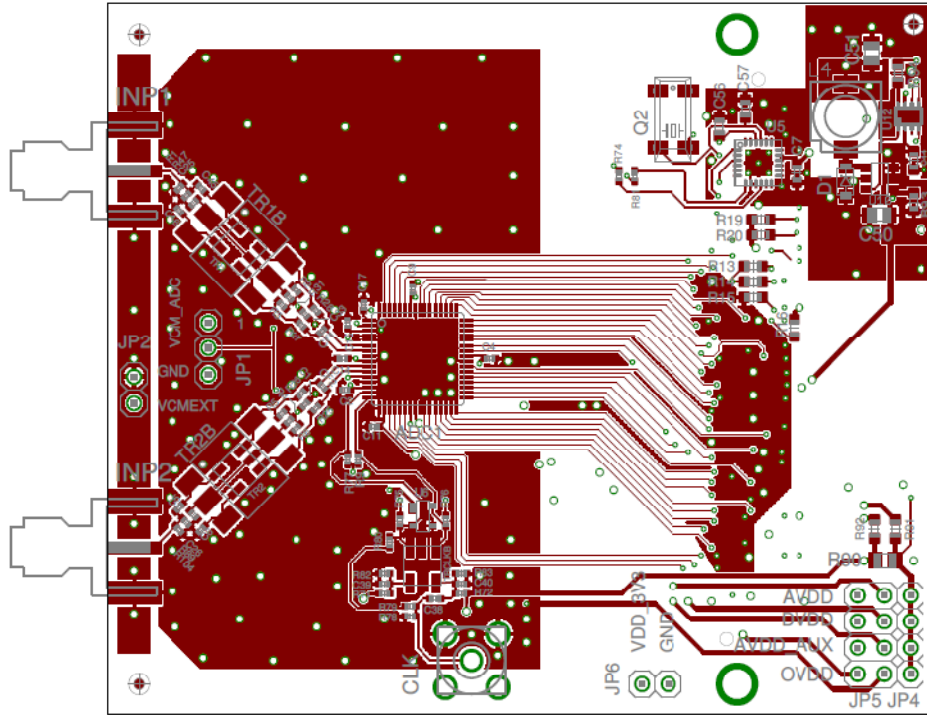




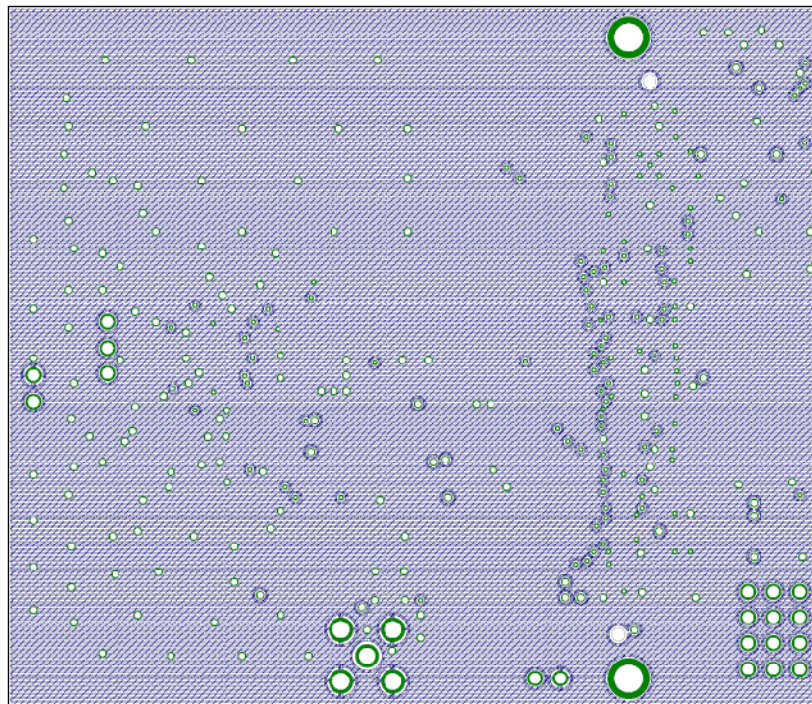
## 11.2 Component placement BOTTOM



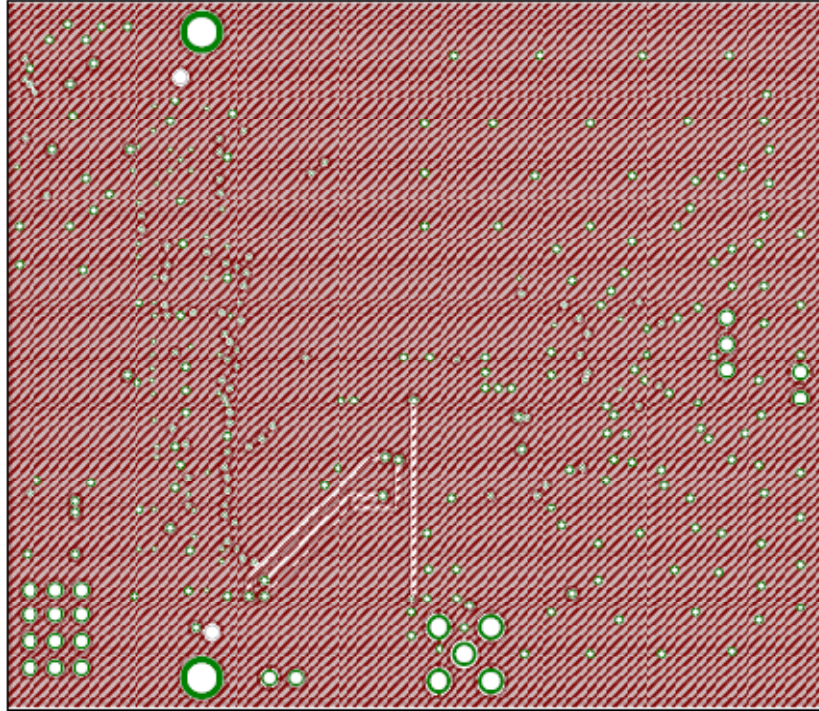
### 11.3 Top layer



### 11.4 Inner layer top



### 11.5 Inner layer bottom



### 11.6 Bottom layer

